

Appl. No. 10/037,729
Amdt. Dated August 17, 2005
Reply to Office action of May 17, 2005
Attorney Docket No. P14604/084845-1051
EUS/J/P/05-6141

REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended Claim 1. Applicant respectfully submits no new matter has been added. Accordingly, Claims 1-40 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Claim Rejections— Obviousness-Type Double Patenting

In paragraph 1 of the Office Action, the Examiner provisionally rejected claims 1, 3-24 and 26-40 under the judicially created doctrine of obviousness-type double patenting over co-pending Application No. 09/972,270. The present application and co-pending Application No. 09/972,270 are commonly owned by the Assignee, Ericsson Inc. To overcome the Examiner's rejection, the Applicant herewith submits a terminal disclaimer. A favorable reconsideration is respectfully requested.

3.) Objected Claims

The Applicant extremely appreciates the Examiner's statement that Claims 11-13, 22-24, and 38-40 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, in view of the above amendments and the following remarks, the Applicant respectfully submits that the pending claims are in condition for allowance and requests the Examiner's favorable reconsideration.

4.) Claim Rejections – 35 U.S.C. § 102(e)

The Examiner rejected claims 1-9 under 35 U.S.C. § 102(e) as being anticipated by Koodli (US 6,608,841). The Applicant respectfully traverses the Examiner's rejection and has further amended independent Claim 1 to more clearly and distinctly claim the subject matter which the Applicant considers as his invention. A favorable reconsideration in view of the above amendments and the following remarks is respectfully requested.

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Unlike a conventional packet communications system wherein a central processor (CPU) would create the header portion of a packet and a digital signal processor (DSP) would create the data portion of the packet, the present applications discloses and claims a method wherein both the header portion as well as the data portion are created by the digital signal processor (DSP). As fully disclosed in the specification, the present invention provides a method for creating a packet, including the necessary headers, in a digital signal processor instead of a CPU where a protocol stack is typically implemented. As a result, the present invention relieves a significant portion of system resources, such as the CPU or the router, from the responsibility of header creation (present application, page 3, paragraph 4). The Applicant respectfully submits that Koodli simply fails to disclose or teach the recited steps of creating both the header portion as well as the data portion by a DSP.

Koodli, on the other hand, merely discloses a compressor or decompressor for providing header compression mechanism in packet creations. However, nowhere in Koodli does it disclose or teach the steps of a digital signal processor (DSP) creating the data portion as well as the header portion of a particular packet. In that regard, the Examiner cited Figs. 2A and 2B of Koodli as allegedly disclosing the recited steps. However, the Applicant respectfully submits that other than generally describing the data structure of a packet (including header portion and payload portion), the Koodli reference is silent on how those portions are actually created. The Applicant further submits that a digital signal processor is not analogous to any other types of general computing processors. As widely used and accepted in the telecommunications industry, the term digital signal processor (DSP) constitutes "a specialized semiconductor device or specialized core in a semiconductor device that processes very efficiently and in real time a stream of digital data that is sampled from analog signals ranging from voice, audio and video and from cellular and wireless to radio and television" (Newton's Telecom Dictionary, 19th Edition, CMP Books). As a result, the Applicant submits that Koodli fails to disclose or teach the steps of creating the data portion as well as the header portion using a DSP as currently claimed.

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The Applicant therefore believes amended independent Claim 1 and its dependent claims are patentable over the cited references.

5.) Claim Rejections – 35 U.S.C. § 103 (a)

The Examiner rejected claims 14-20, 25-29, 31-27 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Koodli in view of James Aweya (XP-004190486 "on the design of IP routers, Part 1: Router architectures", Journal of Systems Architecture, Amsterdam, NL, vol. 46, no. 6, April 2000). The Applicant respectfully disagrees with the Examiner's rejection for at least the same reasons as stated above and submits the following additional remarks.

As fully discussed above, Koodli fails to disclose a DSP creating both the header portion as well as the data portion as recited by the currently pending claims. In that regard, Aweya similarly fails to disclose the novel elements of the present invention. The Aweya reference discloses the basic functionalities associated with IP routers within a communication network. Accordingly, it discloses the basic functionalities of routing packets within a network including packet forwarding (Section 2.2 of Aweya), special router services (Section 2.3), router architecture with a single processor (Section 3.1), bus-based router architecture with multiple processors (Section 3.2), and switched-based router architecture with multiple processors (Section 3.3), etc. However, nowhere in Aweya does it disclose or teach a digital signal processor (DSP) creating the data portion as well as the header portion of a packet. As a matter of facts, packets are already created when it comes into the routers as disclosed in the Aweya reference and the Aweya routers merely look up the header information and appropriately forwards those packets to their intended destinations. In that regard, the Examiner referenced pages 493-502 of the Aweya reference as allegedly disclosing the DSP creating the header portion as well as the data portion as recited by the present pending claims. However, after review of those cited portions of Aweya, the Applicant respectfully submits that other than disclosing the forwarding mechanisms, including cache functions, and different router architectures, Aweya does not disclose or teach the

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novel aspects of creating different portions of a packet using a digital signal processor as claimed.

Accordingly, the Applicant further submits that independent Claims 14 and 26 and their dependent claims are patentable over the cited references and a Notice of Allowance is earnestly requested.

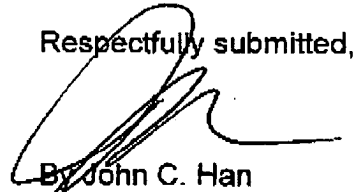
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CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



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